WHAT IS CLAIMED IS:

1.   Switching apparatus operating at a significantly higher data rate than switching elements(SEs) which form a switching fabric and operate at a lower data rate said SEs routing data from at least one ingress source port, which receives data at said higher data rate, to egress destination ports said data being grouped in data packets having a uniform or variable plurality of digital bytes said apparatus comprising:

        a said ingress source port including means for receiving successive data packets at said higher rate and for transmitting data via a plurality of output ports at said lower rate to said SEs ;

        a sequential array of low data rate SEs each having a plurality of input ports individually connected to each said output port of said input source port said SEs and source port including means for switching source output ports successively from one SE to another available SE in response to a data packet event whereby the effective data rate from said source outputs to said SEs is at said higher data rate.

2.   A method of routing data via switching elements(SEs) from ingress source ports which receive data at a significantly higher data rate to egress destination ports, said SEs operating at a lower data rate, said data being grouped in data packets said method comprising the following steps:

        providing a plurality of said SEs in an array which operate at said lower data rate for receiving complete data packets from a said ingress source port and in response to header information carried by said data packet routing such packet to a selected egress destination port:

        a said source port receiving successive data packets at said high rate and sequentially transferring each received data packet at said lower rate to the next available SE whereby the effective throughput of data is at said higher rate and a complete data packet is transmitted through one serial link.

3.   Switching apparatus as in Claim 1 where the ratio of high to low data rates is four to one and where a minimum of four SEs per source port is provided.

4.   Switching apparatus as in Claim 1 where a minimum of two SEs per source port is provided.

5.   Switching apparatus as in Claim 3 where two additional SEs provide for automatic redundancy said switching means being responsive to the failure of an existing SE.

6.   Switching apparatus as in Claim 5 where two additional SEs provide additional bandwidth for overhead.

7.   Switching apparatus as in Claim 1 where the number of SEs is proportional to the ratio of high to low data rates.

8.   Switching apparatus as in Claim 7 where the number of SEs is upwardly scalable to accommodate greater data input.

9.   Switching apparatus as in Claim 1 where said data packet event is the end of one data packet and the beginning of another.

10.   Switching apparatus as in Claim 1 where each data packet is very large in comparison to the number of bytes required for an attached header which identifies such data packet along with its ultimate destination whereby overhead is minimized.